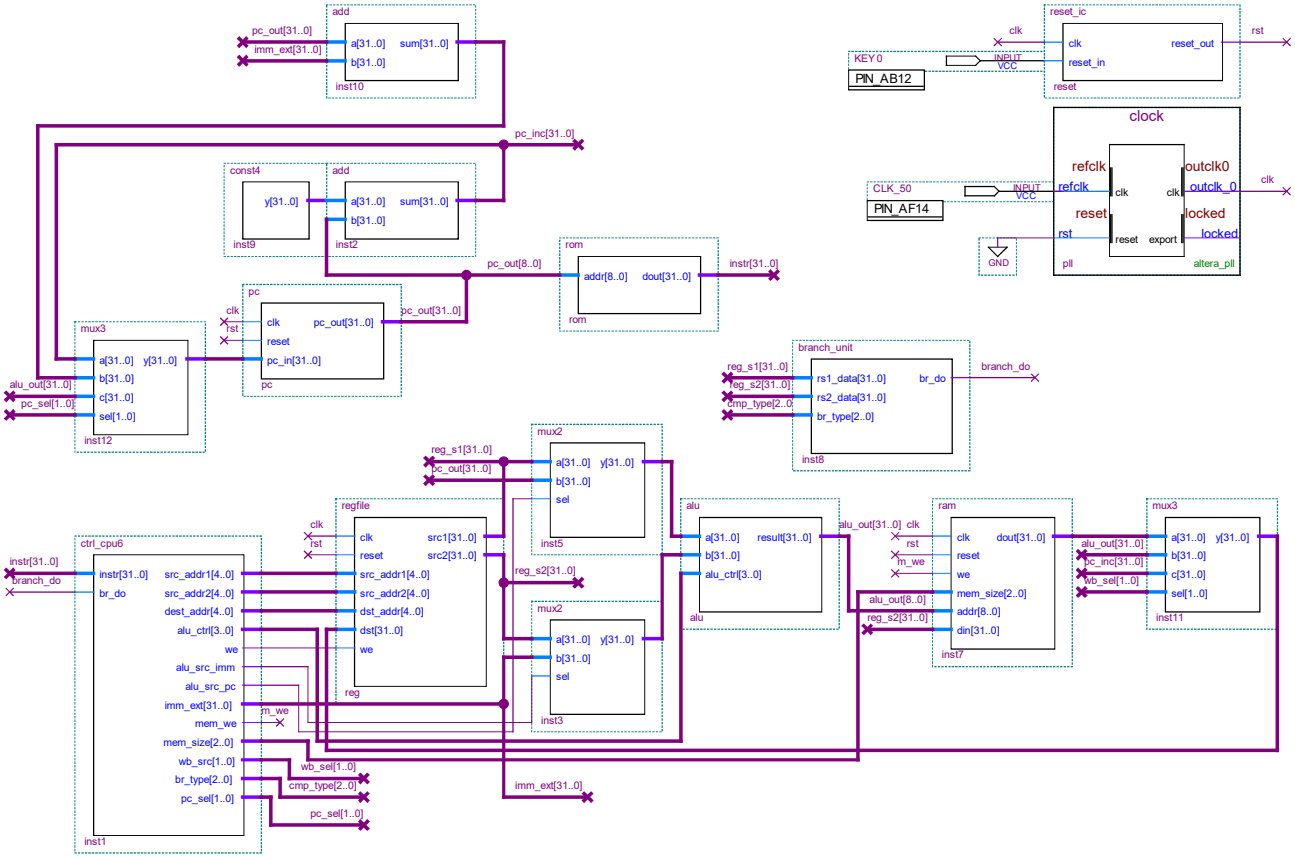
add
pc_out[31..0]
imm_ext[31..0]
a[31..0]
b[31..0]
sum[31..0]
inst10
pc_inc[31..0]
const4
y[31..0]
inst9
inst2
pc_out[8..0]
rom
addr[8..0]
dout[31..0]
instr[31..0]
pc
clk
rst
reset
pc_in[31..0]
mux3
alu_out[31..0]
pc_sel[1..0]
c[31..0]
sel[1..0]
inst12
reset_ic
KEY 0
PIN_AB12
INPUT
VCC
reset_in
reset_out
clock
CLK_50
PIN_AF14
refclk
outclk0
outclk_0
locked
GND
pll
altera_pll
branch_unit
reg_s1[31..0]
reg_s2[31..0]
cmp_type[2..0]
rs1_data[31..0]
rs2_data[31..0]
br_type[2..0]
br_do
branch_do
inst8
mux2
regfile
ctrl_cpu6
src_addr1[4..0]
src_addr2[4..0]
dest_addr[4..0]
alu_ctrl[3..0]
we
alu_src_imm
alu_src_pc
imm_ext[31..0]
mem_we
mem_size[2..0]
wb_src[1..0]
br_type[2..0]
pc_sel[1..0]
wb_sel[1..0]
cmp_type[2..0]
inst1
src1[31..0]
src2[31..0]
dst_addr[4..0]
dst[31..0]
reg
inst5
inst3
alu
result[31..0]
ram
dout[31..0]
addr[8..0]
din[31..0]
mem_size[2..0]
inst7
inst11